

REMARKS

Claims 1-8 and 10-18 are unamended and pending in the application.

For at least the reasons set forth below, withdrawal of all outstanding objections and rejections is respectfully requested.

Entry of Rule 116 Response

Entry of this response is requested because this response does not raise any new issues that would require further consideration and/or search. No new claims are being presented in this response. No new matter is raised by this response. This response could not have been previously presented because the outstanding § 103(a) rejections are based on new reasoning. Lastly, it is requested that the response be entered even if the application is not allowed because this response will place the application in better form for appeal by materially simplifying the issues.

If the application is not in proper form for allowance, Applicants request that the Examiner telephone the undersigned to discuss any further outstanding issues.

Request for Interview Prior to Formal Action on Amendment

Applicants request an interview prior to formal action on this response. An "Applicant Initiated Interview Request Form" accompanies this response. Please contact Applicants' undersigned representative to schedule the interview.

Prior Art Rejections

Claims 1-8 and 11-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,161,097 (Ikeda).

Claims 10 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ikeda in view of U.S. Patent No. 6,975,098 (Vinciarelli).

Claims 16-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ikeda in view of U.S. Patent No. 5,297,203 (Rose).

For the reasons set forth below, all of these rejections are respectfully traversed.

1. Patentability of independent claims 1 and 14 over Ikeda.

Claims 1 and 14 recite, in part, (underlining added for emphasis):

a bypass switch shorting between the input and output of said DC-DC converter; and

a bypass control section maintaining said bypass switch in the ON state during non-operation of said DC-DC converter, and at the start of said switching operation of said DC-DC converter, further maintaining said bypass switch in the ON state for a predetermined time after the start of said switching operation.

Claims 1 and 14 each recite that the bypass control section maintains the bypass switch in the ON state for a predetermined time after the start of the switching operation of the DC-DC converter. This limitation is not disclosed or suggested in Ikeda.

The Examiner states that Fig. 1, items 5, 6 and column 4, lines 13-24 of Ikeda discloses the claimed bypass control section maintaining said bypass switch in the ON state during non-operation of said DC-DC converter, and at a start of said switching operation of said DC-DC converter, further maintaining said bypass switch in the ON state for a predetermined time after the start of said switching operation (column 2, lines 18-22; column 4, lines 42-44). This is incorrect. The Examiner further states that one skilled in the art would recognize that the bypass control circuit comprises a delay to switch off the latching relay 4 only after the DC/DC converter 2 has turned on, in order to maintain continuous power to the load. Applicants respectfully disagree.

Ikeda does not disclose or suggest a bypass control section that maintains the bypass switch in the ON state for a predetermined time after the start of the switching operation of the DC-DC converter, as recited in claims 1 and 14 of the present application. Column 3, line 67 through column 4, line 24 of Ikeda reads as follows: (underlining added for emphasis):

The output voltage V1 of the battery 1 is detected through voltage dividing resistors R3 and R4, and is compared with a reference voltage Vb corresponding to the reference voltage Vs shown in FIG. 2 by a comparator 5. If the output voltage V1 of the battery 1 is higher than the reference voltage Vb, the output signal of the comparator 5 goes HIGH. If

the output voltage V1 of the battery 1 is lower than the reference voltage Vb, the output signal of the comparator 5 goes LOW. The oscillator 25 of the DC-DC converter 2 is controlled by the output signal of the comparator 5. When the output signal of the comparator 5 is HIGH, the oscillator 25 is stopped and the transistor 22 is turned off to hold the DC-DC converter 2 inoperative.

The output signal of the comparator 5 is used also as a control signal for controlling the latching relay 4, i.e., a bypass switch. When the output signal of the comparator 5 is HIGH, a relay controller 6 sets the latching relay 4 to an ON state, and sets the latching relay 4 to an OFF state when the output signal of the comparator 5 is LOW. Thus, the latching relay 4 is set to an ON-state while the output voltage V1 of the battery 1 is higher than the reference voltage Vs to connect the battery 1 directly to the load circuit 3, so that the power of the battery 1 can be supplied to the load circuit 3 without loss.

The DC-DC converter 2 of Ikeda is only operational when the output voltage V1 of the battery 1 is lower than the reference voltage Vb, causing the output signal of the comparator 5 to go LOW. The latching relay 4 is set to an OFF state when the output signal of the comparator 5 is LOW. Thus, unlike the invention recited in claims 1 and 14 of the present application, the latching relay 4 (bypass switch) of Ikeda is not maintained in an ON state for any time after the start of the operation of the DC-DC converter 2. In fact, the simultaneous switching ON of the latching relay 4 (bypass switch) and switching OFF of the DC-DC converter is precisely the deficiency in the prior art that is remedied by the present invention, which maintains the bypass switch in the ON state for a predetermined time after the start of the switching operation (see detailed discussion at page 12, line 2 through page 13, line 21).

Additionally, a person of skill in the art would recognize that it is not desirable to operate both the DC-DC converter and the bypass switch at the same time because their functions conflict with each other to cause energy loss. Thus, conventionally, a bypass switch is turned OFF as soon as the DC-DC converter is turned ON. This is not the same as maintaining said bypass switch in the ON state during non-operation of said DC-DC converter, as recited in claims 1 and 14.

In response to the Applicants' arguments filed December 5, 2006, the Examiner states that Applicants' arguments are equivalent to stating that the Ikeda system is a

break-before-make power supply and would cut off power to the load. This interpretation of Applicants' arguments is incorrect. Applicants' argument is that latching relay 4 of Ikeda is set to an OFF state (break) when the output signal of the comparator 5 is LOW (make). A break-when-make system is not the same as a break-before-make system. On the other hand, the invention of the present application maintains the bypass switch in the ON state during non-operation of the DC-DC converter. To use the Examiner's analogy, it is a break - after - a predetermined time – after - make system.

For the above reasons, Ikeda does not disclose or even remotely suggest the invention recited in claims 1 and 14. In fact, the Ikeda patent teaches away from maintaining the bypass switch in the ON state.

Accordingly, claims 1 and 14 are believed to be patentable over the applied reference.

2. Patentability of the dependent claims

The dependent claims are believed to be patentable over the applied references for at least the reason that they are dependent upon allowable base claims and because they recite additional patentable elements and steps. None of the secondary references make up for (disclose or suggest) the deficiencies of the Ikeda patent as discussed above.

Conclusion

Insofar as the Examiner's rejections were fully addressed, the present application including claims 1-8 and 10-18 is in condition for allowance. Issuance of a Notice of Allowability of all pending claims is therefore requested.

Application No. 10/528,174

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Respectfully submitted,

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April 16, 2007 By: Clark Jablon
(Date)

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